REMARKS

In accordance with the foregoing, the title, specification and claims 1, 10, 17, 18 and 22-28 are amended. New claim 29 is presented.

No new matter is presented in any of the foregoing and, accordingly, approval and entry of the amended title, specification, claims and new claims are respectfully requested.

TRAVERSE OF 35 U.S.C. §102(b) AND 35 U.S.C. §103(a) REJECTIONS

Independent claim 1, 27, 28 all as amended, recites a processor control apparatus for controlling a plurality of arithmetic units, a processor, and a method, respectively, using claim 1 as an example, including a "plurality of instruction control units issuing a series of instructions to said plurality of arithmetic units, wherein at least one of said instruction control units switches between a first execution process driving said plurality of arithmetic units by a single series of instructions issued from one of the plurality of instruction control units and a second execution process correspondingly driving said plurality of arithmetic units by a plurality of different series of instructions issued respectively from said plurality of instruction control units."

Independent claims 10, 17, 24, 25, all as amended, using claim 10 as an example, recite a processor control apparatus "wherein said plurality of series of instructions are issued to said plurality of arithmetic units from one of the plurality of instruction memories or are issued respectively from said plurality of instruction memories to enable said plurality of arithmetic units to be simultaneously and independently driven."

Independent claims 18, 22, 26, all as amended, recite, using claim 18 as an example, an apparatus wherein "from a first instruction memory of one of said instruction control units simultaneously driving the plurality of arithmetic units and a second series of instructions from a second instruction memory of another instruction control unit different from said one instruction control unit independently driving each of the plurality of arithmetic units to output one of said first and second series of instructions thus selected to said instruction decoder."

Independent claim 23 recites a processor " wherein some of said instruction control units are operable to switch between a first execution process for synchronous driving said plurality of arithmetic units by a single series of instructions and a second execution process independently driving said plurality of arithmetic units by a plurality of different series of instructions, respectively, wherein the synchronous driving and the independent driving."

Applicants submit that these features are not discussed by the art relied on by the Examiner, either alone or in combination.

In contrast to the art relied on by the Examiner, either alone or in combination, aspects of the present invention enable switching between simultaneously driving arithmetic units by issuing a single series of instructions (SIMD) from a instruction control unit and independently driving the arithmetic units by correspondingly issuing series of instructions (VLIW) from respective instruction control units connected with the arithmetic units.

Applicants submit that Parady (U.S.P. 5,933,627) does not discuss switching between simultaneously driving arithmetic units by issuing a single series of instructions from a instruction control unit and independently driving the arithmetic units. Rather, Parady merely discusses handling blocked memory accesses of a program resulting from accesses to the memory that require waiting by switching between threads of the program.

According to Parady, instructions are provided to an instruction buffer to be accessed by a dispatch unit (see, col. 3, lines 10-12). The dispatch unit includes an instruction cache and instruction buffers corresponding to a number of threads of the instruction, for example, four instruction buffers for each of the 0-3 threads (see, col. 5, lines 8-10). Similarly, integer register and floating point register files are also divided up into four register files to support threads 0-3 (see, col. 3, lines 35-43). Then, upon an indication that a thread switch is required, a switch to the next thread is performed (see, col. 3, lines 57-65). Thus, Parady discusses merely limitations to switchably executing portions or threads of a program responsive to an event.

Fernando (U.S.P. 6,272,616) does not discuss a "plurality of series of instructions are issued to said plurality of arithmetic units from one of the plurality of instruction memories or are issued respectively from said plurality of instruction memories to enable said plurality of arithmetic units to be simultaneously and independently driven."

Fernando merely discusses a digital processor alternatively operating in a single threaded mode, a single instruction mode and a multiple instruction mode. Rather, Fernando discusses that in response to a CFORK instruction, a control signal instructs a multiplexer to accept data from input line (36) from a fetch stage of a primary instruction pipeline, and a decoder in a secondary instruction pipeline is activated (see, col. 6, lines 40-50). Then, the secondary instruction pipeline commences to execute the code fetched by fetch stage while primary instruction pipeline continues to execute the same instructions (see, col. 6, lines 51-54). On the other hand, in response to a DFORK instruction, the state machine issues signals instructing the multiplexer to accept instructions from fetch stage through input line (35) (see, col. 7, 12-35). Then, the two threads (16 and 18) will operate essentially independently of each other, reading and executing different instructions and using different data (see, col. 7, lines 36-

38).

Dowling (U.S.P. 6,170051) does not discuss that a "plurality of series of instructions are issued to said plurality of arithmetic units from the instruction memory to be simultaneously and independently driven."

Rather, Dowling merely discusses very long instruction word (VLIW), a microprocessor design technology, and a chip capable of executing many operations within one clock cycle to reduce program instructions into basic operations that the processor can perform simultaneously. (See, for example, col. 3, starting at line 7). The operations are put into a very long instruction word that the processor then takes apart and passes the operations off to the appropriate devices. This enables the present invention to control a processor of an apparatus, such as a built-in device, etc., without consuming much power by reducing clock frequency resulting from executing control of the apparatus.

Applicants submit that an *arguendo* combination of any of the art relied on by the Examiner does not teach for example, an apparatus "wherein said plurality of series of instructions are issued to said plurality of arithmetic units from one of the plurality of instruction memories or are issued respectively from said plurality of instruction memories to enable said plurality of arithmetic units to be simultaneously and independently driven."

Rather, an *arguendo* combination of Parady in view of Dowling merely teaches switching between threads in response to a long-latency event, and an enhanced VLIW architecture. An *arguendo* combination of Parady in view of Fernando teaches switching between threads in response to a long-latency event including a method to switch between a scalar command (SINGLE), an SIMD command, and an MIMD command. An *arguendo* combination of Fernando in view of Dowling teaches a method to switch between a scalar command (SINGLE), an SIMD command, and an MIMD command, and an enhanced VLIW architecture. An *arguendo* combination of Fernando in view of Parady teaches method to switch between a scalar command (SINGLE), an SIMD command, and an MIMD command and switching between threads in response to a long-latency event

Conclusion

Since features recited by the independent claims (and claims dependent thereon) are not discussed by the art relied on by the Examiner, either alone or in combination, the rejections should be withdrawn and claims 1-28 allowed.

NEW CLAIM

New claim 29 recites a processor control method to control a plurality of arithmetic units connected with a plurality of instruction control units, comprising "switching between simultaneously driving the plurality of arithmetic units by issuing a single series of instructions from one of the plurality of instruction control units and independently driving each of the plurality of arithmetic units by correspondingly issuing series of instructions from the plurality of instruction control units, wherein the switching is performed based on contents of processes to be executed."

These, features of claim 29 patentably distinguish over the cited art, and they are submitted to be allowable for the recitations therein.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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